THAT WHICH IS CLAIMED:

1. A delay-locked loop (DLL) circuit, comprising:

a phase interpolator circuit and variable delay circuit coupled in cascade and operative to generate an output clock signal that is delayed with respect to a reference clock signal responsive to respective first and second control signals applied to the phase interpolator and the variable delay circuit; and

a phase control circuit that generates the first and second control signals responsive to the output clock signal and the reference clock signal.

2. A DLL circuit according to Claim 1, wherein the variable delay circuit provides a coarser resolution than the phase interpolator circuit.

3. A DLL circuit according to Claim 1, wherein the variable delay circuit is configured to provide step changes in delay responsive to the second control signal.

4. A DLL circuit according to Claim 3, wherein the variable delay circuit comprises a tapped delay chain circuit comprising a plurality of delay circuits interconnected by a switching circuit that is operative to selectively bypass one or more of the delay circuits responsive to the second control signal.

5. A DLL circuit according to Claim 1, wherein the phase control circuit is operative to cause the phase interpolator circuit to shift from one extreme of a delay range thereof towards another extreme of the delay range concurrent with a step change in delay through the variable delay circuit.

6. A DLL circuit according to Claim 1, wherein the phase interpolator circuit comprises:

first and second delay circuit coupled in series and generating respective first and second delayed clock signals; and

a phase interpolator that receives the first and second delayed clock circuits and that generates a phase interpolated clock signal therefrom.

7. A DLL circuit according to Claim 6, wherein the phase interpolator comprises one of an analog phase interpolator or a digital phase interpolator.

8. A DLL circuit according to Claim 1, wherein the phase interpolator circuit receives the reference clock signal and produces a phase interpolated clock signal therefrom, and wherein the variable delay circuit receives the phase interpolated clock signal and generates the output clock signal therefrom.

9. A DLL circuit according to Claim 1, wherein the variable delay circuit receives the reference clock signal and produces a variably delayed clock signal therefrom, and wherein the phase interpolator circuit receives the variably delayed clock signal and generates the output clock signal therefrom.

10. A DLL circuit according to Claim 1, wherein the phase control circuit comprises:

a phase detector that generates an error signal responsive to a comparison of the reference clock signal to the output clock signal; and

a delay control circuit that generates the first and second control signals responsive to the error signal.

11. A DLL circuit according to Claim 10:

wherein the delay control circuit comprises:

a fine control counter circuit that increments and decrements a fine control count signal responsive to the error signal and that generates a count limit indicator signal responsive to the fine control count signal reaching one of a maximum or minimum count; and

a coarse control counter circuit that increments and decrements a coarse control count signal responsive to the error signal subject to the count limit indicator signal;

wherein the phase interpolator circuit is responsive to the fine control count signal; and

wherein the variable delay circuit is responsive to the coarse control count signal.

12. A DLL circuit according to Claim 11, wherein the coarse control counter circuit is enabled to count responsive to assertion of the count limit indicator signals.

13. A DLL circuit according to Claim 11, wherein the error signal comprises first and second error signals, wherein the fine control counter circuit increments and decrements responsive to respective ones of the first and second error signals, and wherein the coarse control counter circuit increments and decrements responsive to respective ones of the first and second error signals.

14. A DLL circuit, comprising:

a cascade combination of a phase interpolator circuit and a tapped delay chain circuit, the cascade combination operative to produce an output clock signal that is delayed with respect to a reference clock signal responsive to a control input; and

a phase control circuit that generates the control input responsive to a comparison of the output clock signal to the reference clock signal.

15. A DLL circuit according to Claim 14, wherein the phase interpolator circuit is configured to provide a fine delay adjustment and wherein the tapped delay chain is configured to provide a coarse delay adjustment.

16. A DLL circuit according to Claim 14, wherein the tapped delay chain circuit comprises a cascade of selectively bypassable fixed delay circuits.

17. A DLL circuit according to Claim 14, wherein a delay resolution of the tapped delay chain circuit is substantially the same as a delay range of the phase interpolator circuit.

18. A DLL circuit according to Claim 14, wherein the phase control circuit is operative to cause the phase interpolator circuit to shift from one extreme of a delay range thereof towards another extreme of the delay range concurrent with a step change in delay through the tapped delay chain circuit.

19. A DLL circuit according to Claim 14, wherein the phase interpolator circuit comprises:

cascaded first and second delay circuits that generate respective first and second delayed clock signals; and

a phase interpolator that receives the first and second delayed clock signals and that generates a phase interpolated clock signal therefrom.

20. A DLL circuit according to Claim 19, wherein the phase interpolator comprises one of an analog phase interpolator or a digital phase interpolator.

21. A DLL circuit according to Claim 14, wherein the phase interpolator circuit precedes the tapped delay chain circuit.

22. A DLL circuit according to Claim 14, wherein the tapped delay chain circuit precedes the phase interpolator circuit.

23. A DLL circuit according to Claim 14, wherein the phase control circuit comprises:

a phase detector circuit that generates that generates an error signal responsive to a comparison of the reference clock signal to the output clock signal; and

a delay control circuit that generates the first and second control signals responsive to the error signal.

24. A DLL circuit according to Claim 23:

wherein the delay control circuit comprises:

a fine control counter circuit that increments and decrements a fine control count signal responsive to the error signal and that generates respective minimum and maximum count limit indicator signals responsive to the fine control count signal reaching respective ones of maximum and minimum counts; and

a coarse control counter circuit that increments and decrements a coarse control count signal responsive to the error signal subject to the maximum and minimum count limit indicator signals;

wherein the phase interpolator circuit is responsive to the fine control count signal; and

wherein the tapped delay chain circuit is responsive to the coarse control count signal.

25. A DLL circuit according to Claim 24, wherein the coarse control counter circuit is enabled responsive to assertion of one of the maximum and minimum count limit indicator signals.

26. A DLL circuit according to Claim 24, wherein the error signal comprises first and second error signals, wherein the fine control counter circuit increments and decrements responsive to respective ones of the first and second error signals, and wherein the coarse control counter circuit increments and decrements responsive to respective ones of the first and second error signals.

27. A method of synchronizing an output clock signal to a reference clock signal, the method comprising:

applying the reference clock signal to a cascade combination of a phase interpolator and a tapped delay chain circuit to generate an output clock signal; and

controlling the phase interpolator and the tapped delay chain circuit responsive to a comparison of the reference clock signal and the output clock signal.

28. A method according to Claim 27, wherein controlling the phase interpolator and the tapped delay chain circuit comprises providing fine delay control using the phase interpolator and providing coarse delay control using the tapped delay chain circuit.